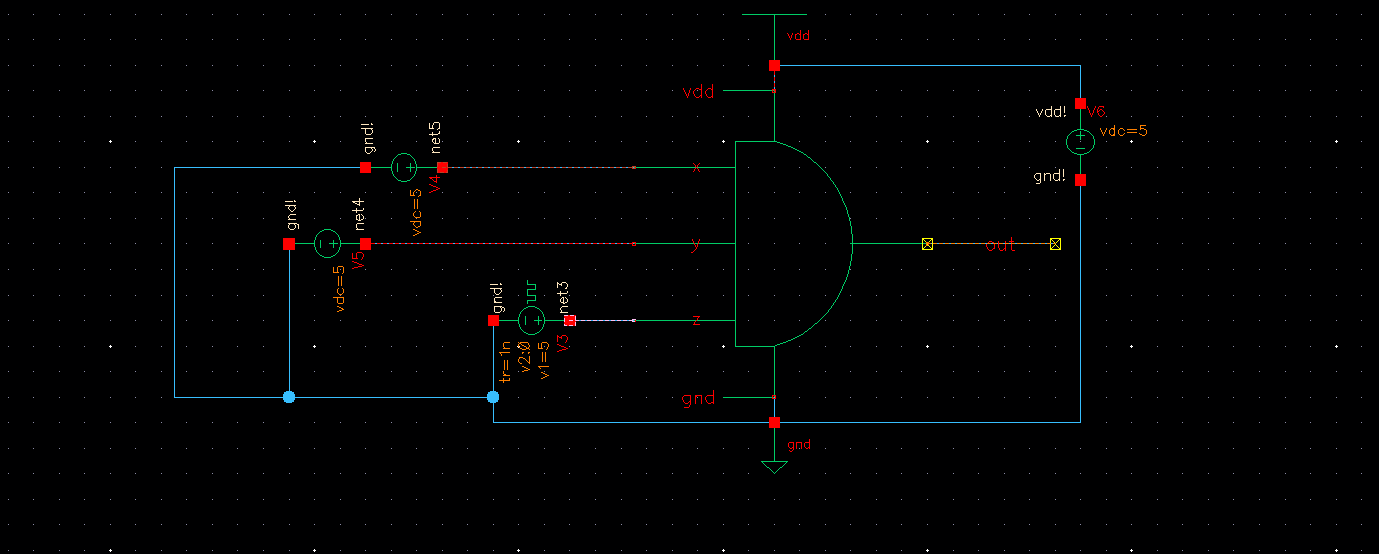
Jomar Pueyo UXT302

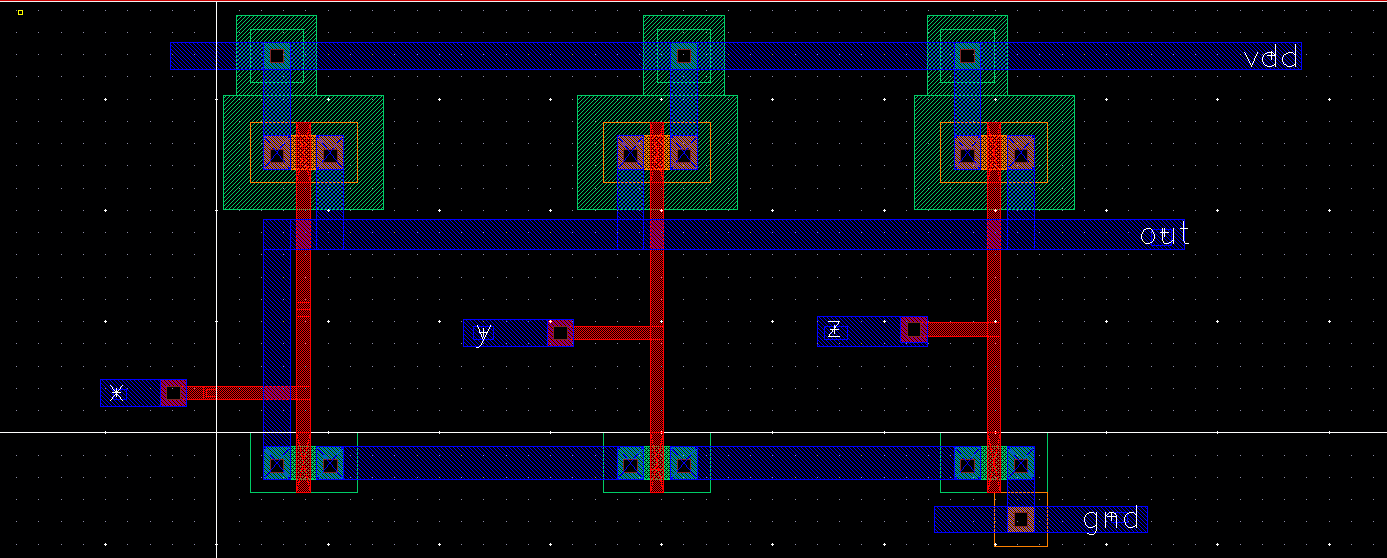
**Lab Assignment 5 – Cadence Layout Assignment**

**3-Input NAND Gate**

Schematic:

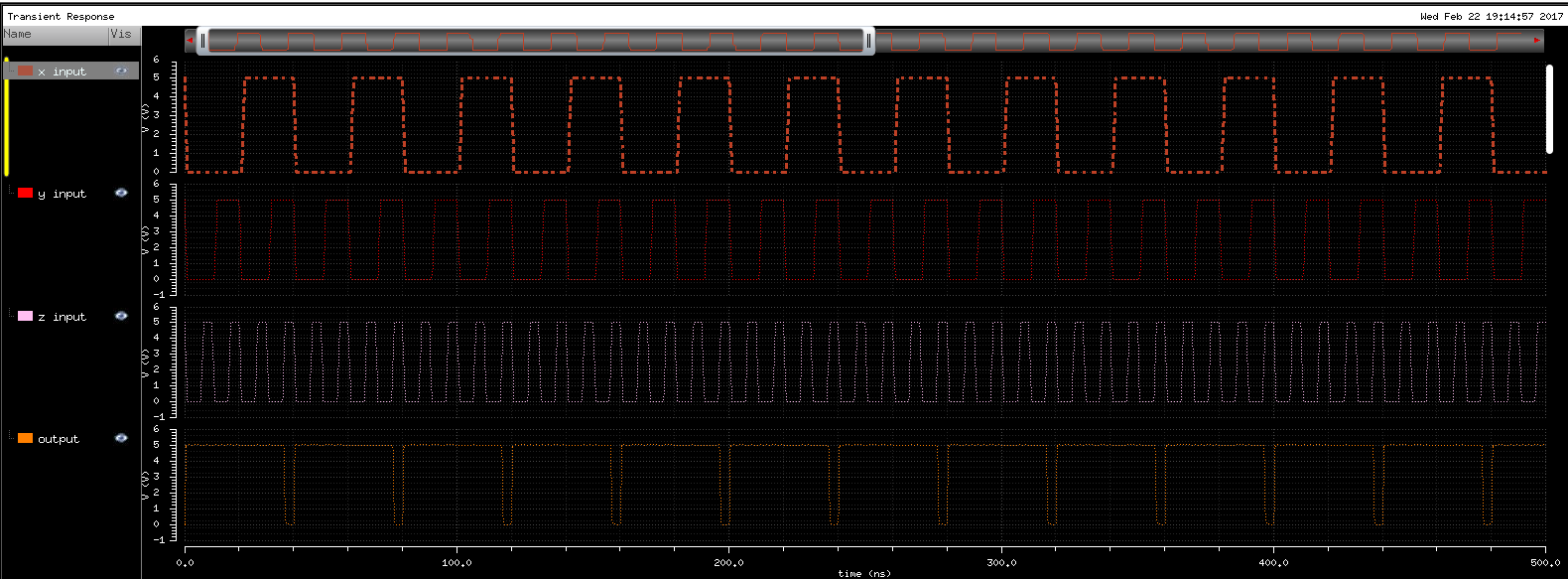


Layout:



* 6 Total Transistors used in this layout: 3 PMOS, 3NMOS
* In the NAND layout all the NMOS transistors are in series with each other while the PMOS transistors are in parallel.

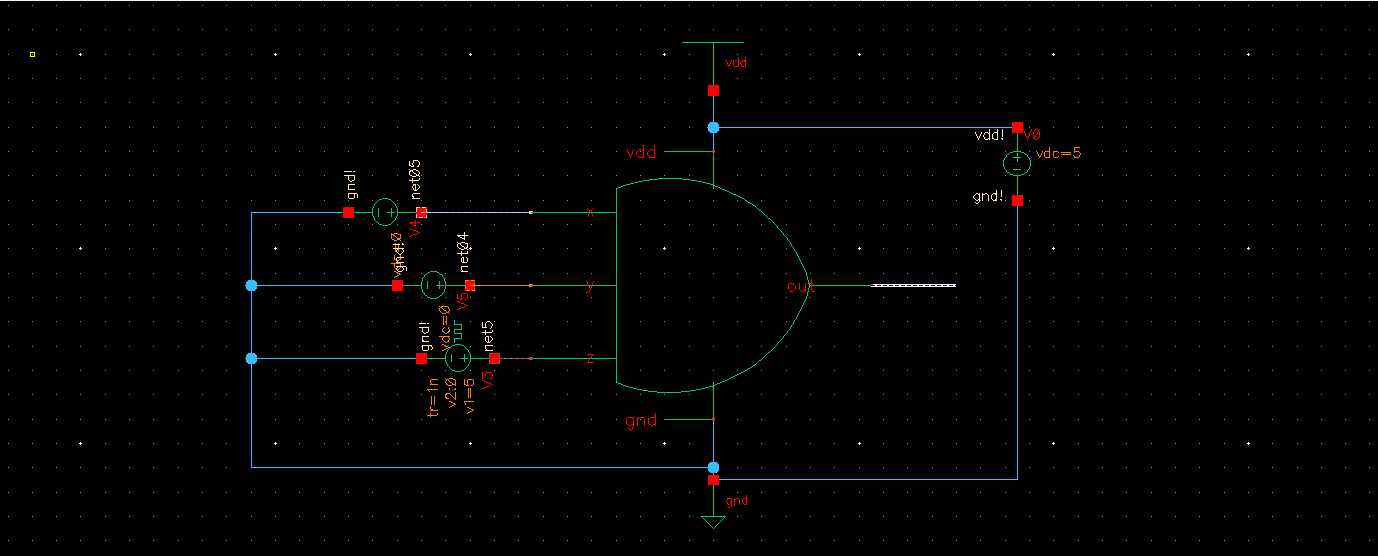
Waveform:



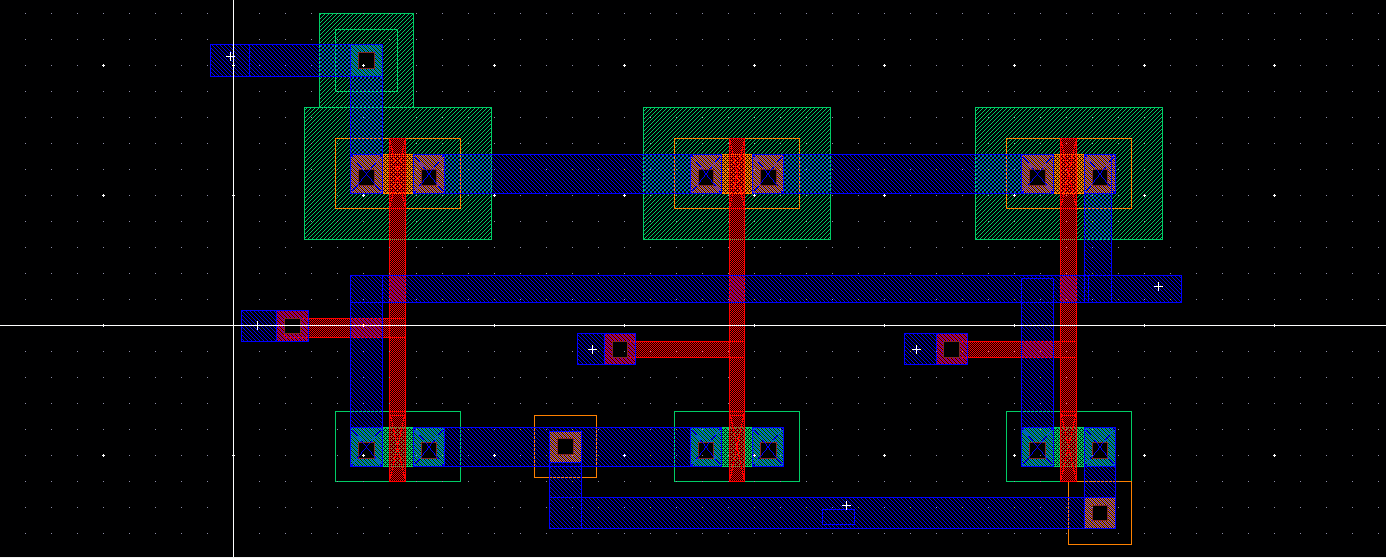
* The output only goes low when all values of X ,Y, and Z are all high which behaves as a NAND gate

**3-Input NOR Gate**

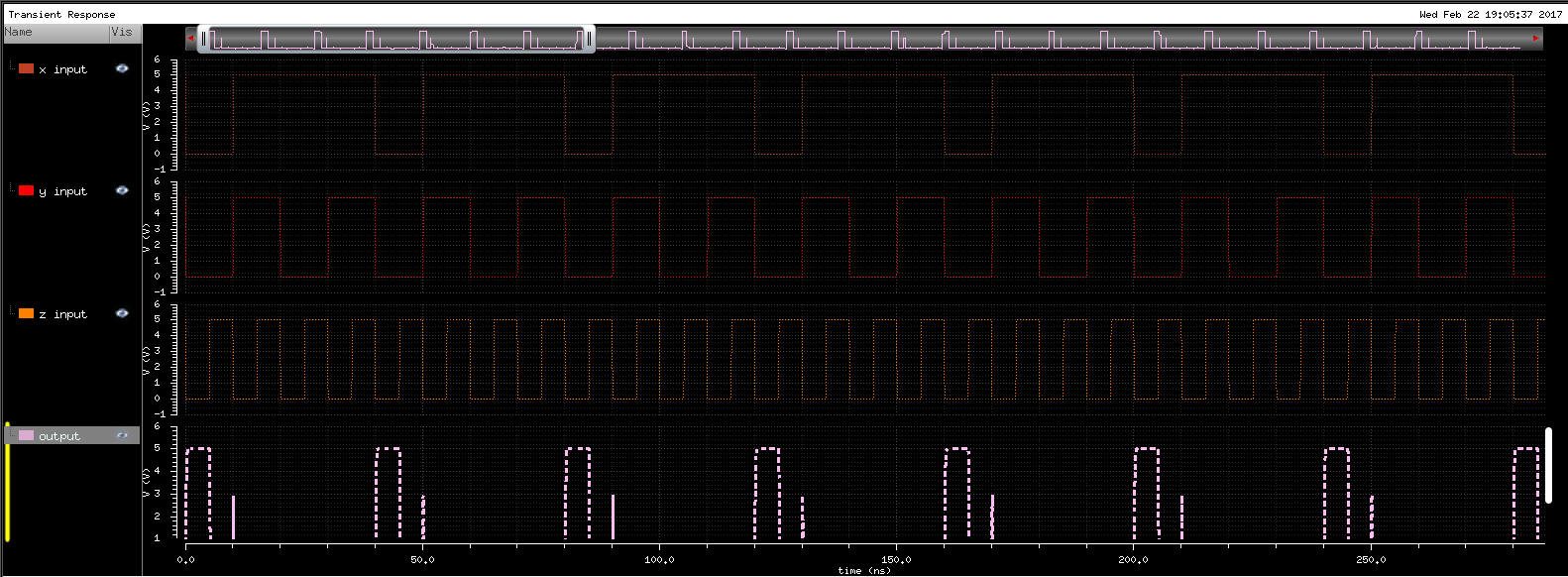
Schematic:



Layout:



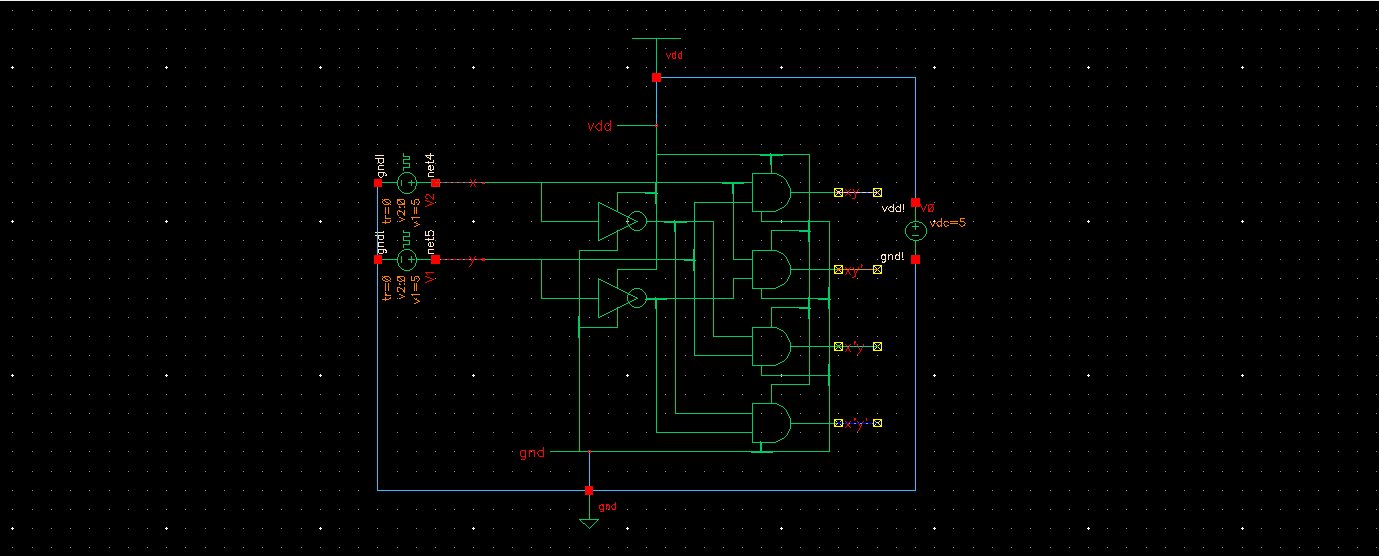
* 6 Total Transistors used in this layout: 3 PMOS, 3NMOS
* In this NOR layout the PMOS transistors are all in series while the NMOS transistors are in parallel.

Waveform:  


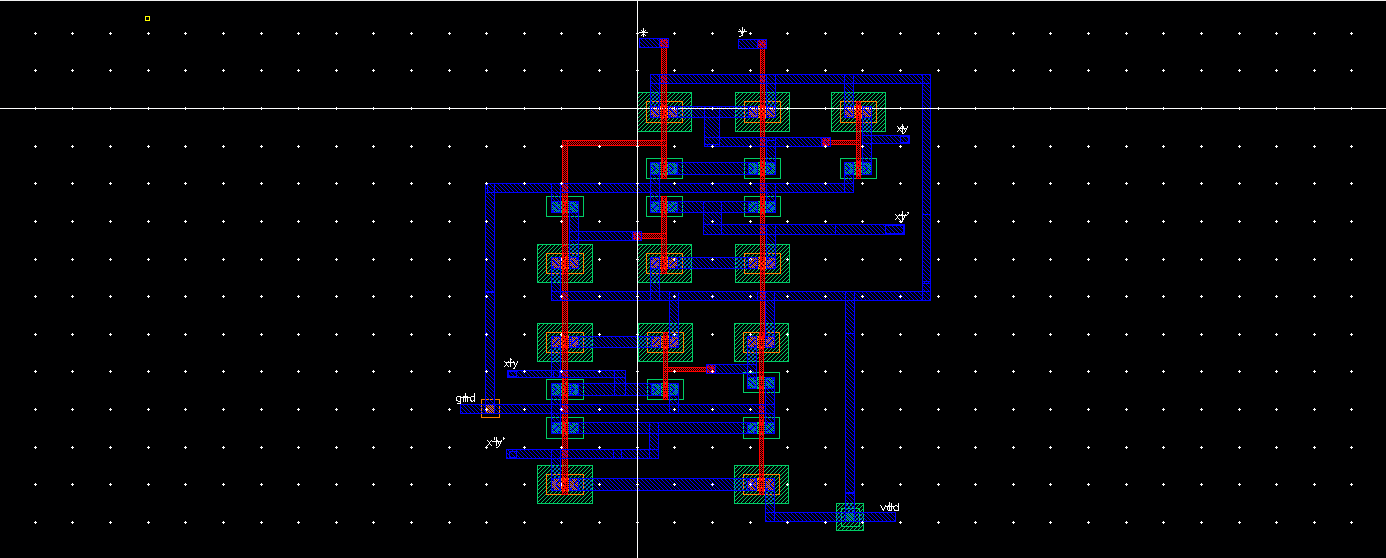
* The output only goes high when all values are low, thus a NOR gate.
* There is a short time when the output goes high due to the Z output transitioning from high to low while both X and Y are going high. This is due to the rise and fall times mismatching.

**2 to 4 Multiplexer**

Schematic:

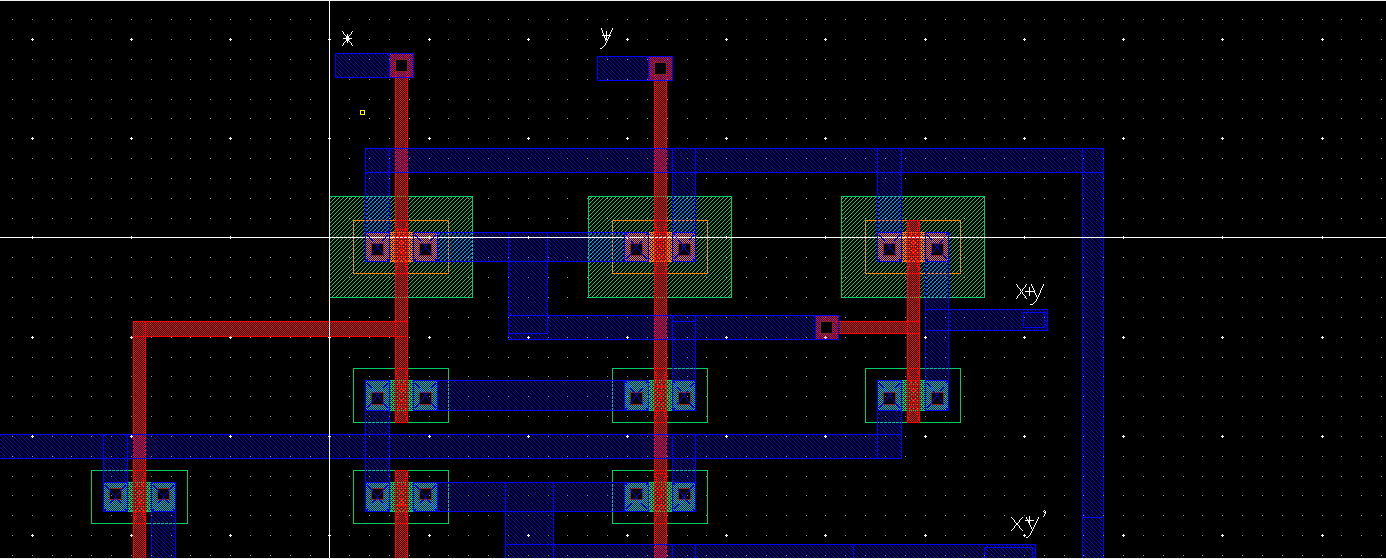


Layout:



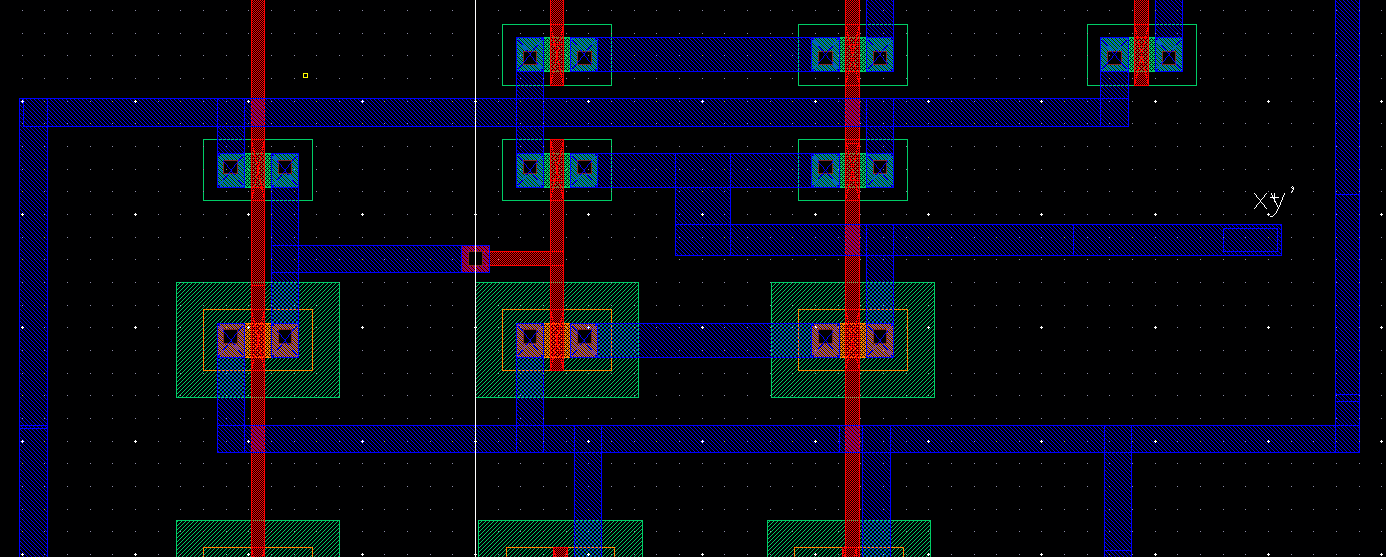
* 22 Total Transistors used in this layout: 11 PMOS, 11 NMOS
* In this layout all the outputs are divided into 4 outputs sections
* The upper most section is the XY output
* The 2nd section is the XY’ output
* The 3rd section is the X’Y output
* The bottom most section is the X’Y’ output
* There is only one source of GND and VDD with the X and Y inputs at the top

XY Output:



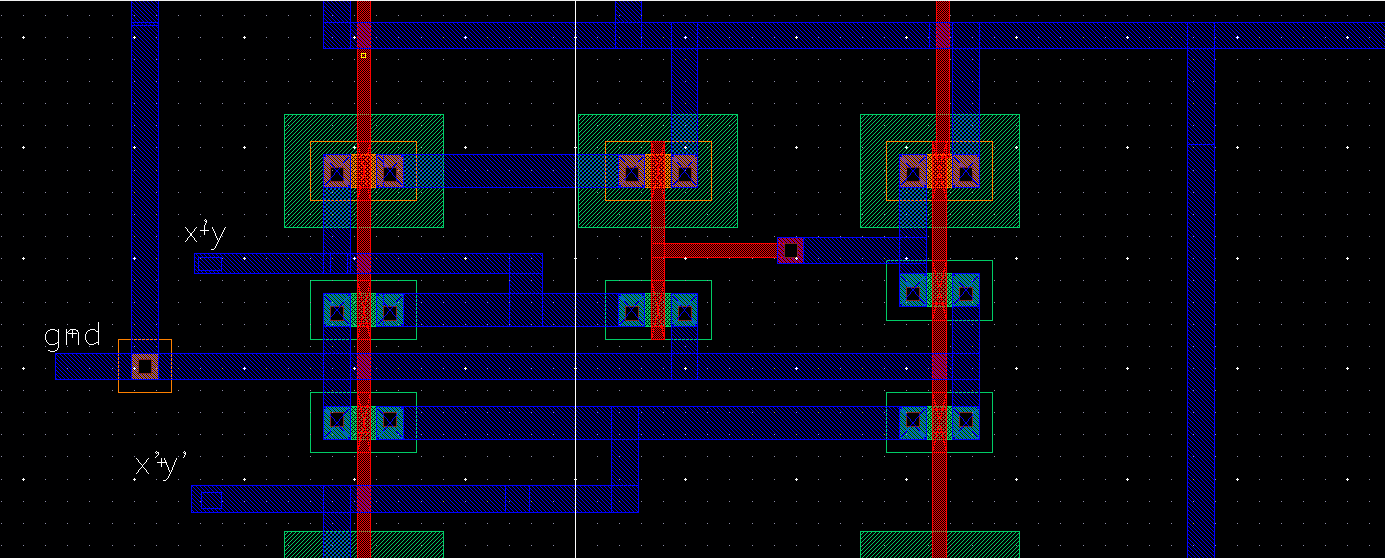
* The XY Output consists of an inverse of the NAND gate
* This section uses 6 Transistors: 3 PMOS, 3 NMOS
* From left to right, NAND gate into Inverter

XY’ Output:



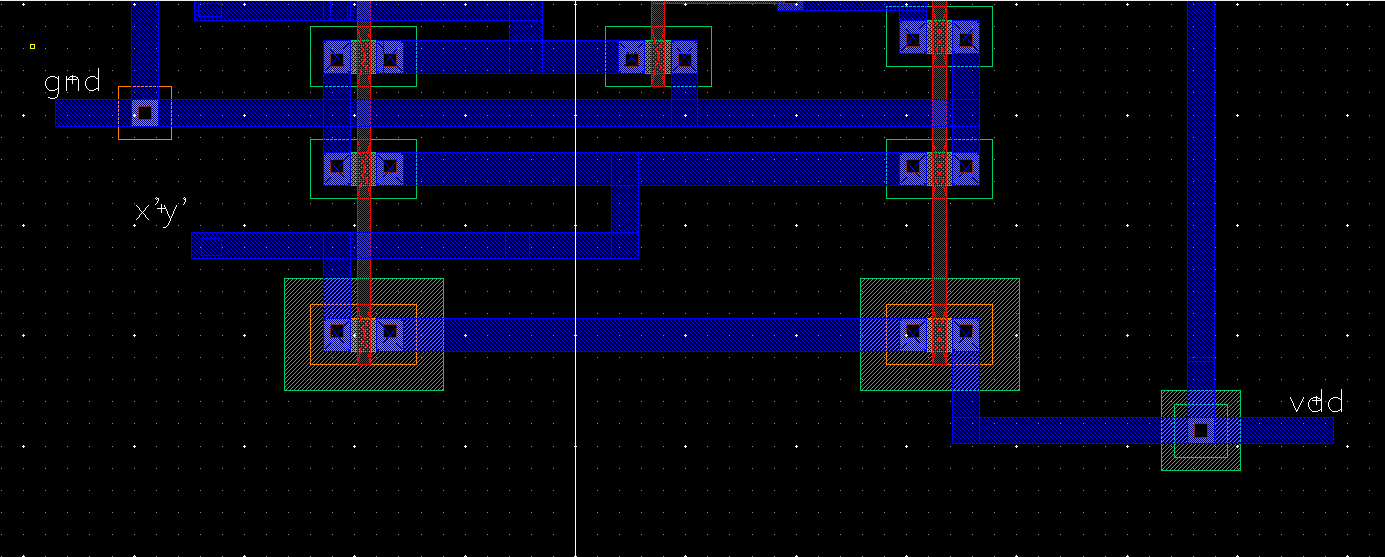
* The XY’ Output consists of an inverted X input NOR gated together with Y
* This section uses 6 Transistors: 3 PMOS, 3 NMOS
* From left to right, Inverted X into NOR gate

X’Y Output:



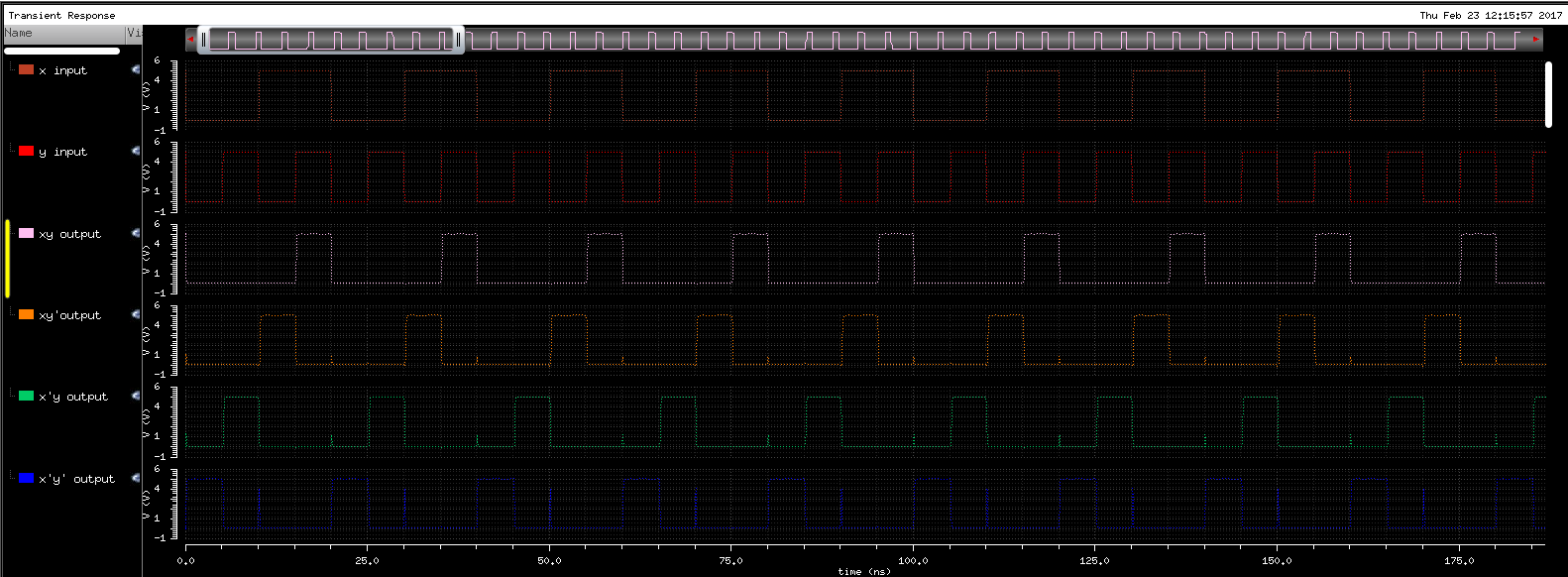
* The XY’ Output consists of an inverted Y input NOR gated together with X
* This section uses 6 Transistors: 3 PMOS, 3 NMOS
* From right to left, Inverted Y into NOR gate

X’Y’ Output:



* The X’Y’ Output is just a NOR gate
* This section uses 4 Transistors: 2 PMOS, 2 NMOS

Waveform:



* The waveform acts as a multiplexer
* XY output only goes high when X=1 and Y=1
* XY’ output only goes high at X=1 and Y=0
* X’Y output only goes high at X=0 and Y=1
* X’Y’ output only goes high at X=0 and Y=0
* There are bits where rise/fall time between X and Y causes some of the outputs to rise for a short time

While creating this layout I have noticed there are better ways to implement this that gives the same results, reduces transistor amount, and reduces layout area by combining transistors and creating series inputs or outputs. In the future I will try to attempt to better my design.